Amendments to the Specification:

Please replace the paragraph beginning at line 7 on page 3 of the specification with the following amended paragraph:

In the case of many loads distributed spatially along a power distribution bus constituting the distribution network, remote sensing ~~can not~~ cannot eliminate the problem for all of the loads because the sensing takes place only at one point along the distribution bus. In the case of loads distributed in two or three dimensions, for example several loads constituted by integrated circuits on a printed circuit board (PCB), remote sensing can reduce the problem of power supply voltage regulation to a degree, but it ~~can not~~ cannot fully compensate at all load points.

Please replace the paragraph beginning at line 17 on page 3 of the specification with the following amended paragraph:

This problem increases as power supply voltages decrease and as current increases, as is the present trend for power supply voltages for digital integrated circuits. For example, with progressively higher resolution integrated circuit technology (e.g. 0.35 μm down to about 1 μm and less) ~~it is necessary to reduce~~ power supply voltages are reduced (e.g. from about 3.3 volts to about 1.0 volt or less) in order to avoid problems such as tunneling effects and electrical field breakdown. The lower the power supply voltage, the greater is the relative proportion of a given voltage drop in the power distribution network. Further, such lower power supply voltages may typically be accompanied by corresponding increases in load current, further increasing the voltage drops in the power distribution network.

Please replace the paragraph beginning at line 1 on page 4 of the specification with the following amended paragraph:

This problem is further increased in situations where the power distribution network uses conductors with a relatively high resistance[[; for]]. For example this may be the case for distribution of power across the surface of a silicon integrated circuit die, or in a multi-layer PCB in which the thickness of copper layers, including power and ground planes or layers, may be restricted by the number of layers and by minimum trace width requirements. The resistance of the power and ground planes may be further increased by the interruption of these planes by many vias in the PCB.

Please replace the paragraph beginning at line 11 on page 4 of the specification with the following amended paragraph:

A known approach to reducing this problem is to use large, low-resistance conductors to distribute power. For example, on a circuit card a plurality of spaced bus bars of substantial size and relatively low resistance may be provided ~~extending~~ . These bus bars may extend across the card to convey the power supply voltage to multiple points on the card[[, the]]. The bus bars ~~being~~ are supplied with the power supply voltage from the power source, for example a regulated voltage power supply on the circuit card, via a further bus bar also of substantial size and positioned at an edge of the card. On a smaller scale, within an integrated circuit, multiple bond wire connections can be provided around the edge of the power plane and, in some cases, to wire-bond to the power plane at interior points of the integrated circuit.

Please replace the paragraph beginning at line 28 on page 4 of the specification with the following amended paragraph:

It is also known, for current sharing purposes and especially to provide redundancy of power supplies in electrical equipment, to provide two power supplies for supplying a power supply voltage to a power supply voltage path. For example, in an equipment rack with a back-plane carrying such a power supply voltage path for connection to a plurality of circuit cards which may be inserted into sockets on the back-plane, a regulated voltage power source may be provided at each side of the equipment rack, i.e. at each end of the power supply voltage path[[, and a]]. A voltage sensing point for use in a feedback control loop of the power sources may be provided at a mid-point of the power supply voltage path. In normal operation of such an arrangement load current for other circuit cards connected to the back-plane is shared between the two regulated voltage power sources, and the presence of the two power sources provides redundancy for the power supply. Such an arrangement does not provide a solution for the problem discussed above.

Please replace the paragraph beginning at line 15 on page 9 of the specification with the following amended paragraph:

The PCB 10 is a multi-layer board, including at least one ground plane and at least one power plane as well as one or more signal planes, arranged in multiple layers in ~~known manner~~ a known manner. The power plane provides a supply voltage to the ICs, and the ground plane provides a return path for this supply, whereby the ICs are supplied with power at the desired supply voltage from the power sources. Accordingly, via the power plane and the ground plane all of the power sources PS0 to PS4 are effectively connected in parallel for providing substantially the same supply voltage to all of the ICs, also connected in parallel.

Please replace the paragraph beginning at line 10 on page 12 of the specification with the following amended paragraph:

Fig. 3 schematically illustrates an equivalent circuit of the distribution network constituted by the power sources PS0 to PS4, each of which is a regulated current source as illustrated in Fig. 3, integrated circuit loads IC0 to IC4, and power supply paths constituted by the power and ground planes of the PCB 10 in Fig. 2. As illustrated in Fig. 3, each of the power sources PS0 to PS4 is connected to each of the ICs IC0 to IC4 via a respective resistor R00 to R04, R10 to[[R04]] R14, ... R40 to R44. In each case the resistor R00 to R44 represents as a lumped element the total resistance, between the power source and the load, of the power supply path and return path via the power and ground planes. This total resistance also includes, for example, resistance of vias for the power and ground plane connections and any short track on an outer layer of the PCB for connection to the IC, for example in the case of surface mount ICs.

Please replace the paragraph beginning at line 10 on page 13 of the specification with the following amended paragraph:

Referring to Fig. 4, the power and ground planes of the PCB 10 are represented by parallel connection buses 20 and 22 respectively. A plurality of loads 24, corresponding to the ICs as described above, are each connected to the buses 20 and 22 at respective points to receive a supply voltage. A plurality of current sources 26, corresponding to the power sources as described above and each providing a regulated current, have their outputs connected at respective points to the buses 20 and [[24]]22 to provide a power supply thereto. Voltage is sensed at a point 28 along the buses 20 and 22, representing voltage sensing at a desired location in the two dimensions of the PCB 10, by conductors 30 connected to the buses 20 and 22 at this point. The conductors 30 are connected to voltage sense input circuits 27 of each of the current sources 26 as a feedback control signal for controlling the output current of the respective current source 26.

Please replace the paragraph beginning at line 24 on page 14 of the specification with the following amended paragraph:

It can be appreciated that as described above the power supply distribution network provides an active current sharing arrangement in accordance with which the currents produced by the current sources 26, constituting the power sources PS0 to PS4, are controlled to maintain the voltage sensed at each sensing point at the desired level, the currents supplied by the current sources being maintained substantially equal or in accordance with a desired weighting. This has the effect of slightly raising the voltage between the power and ground planes in regions of the PCB 10 where loads are drawing a reduced power, lowering the voltage in regions where loads are drawing more power, and maintaining a more even current flow in different regions. This reduces the difference between maximum and minimum currents in the network, and therefore reduces the difference between maximum and minimum voltage~~; thus it reduces supply~~. Supply voltage variation over the PCB 10 as a whole is thus reduced.